

4222635/C 01/2018

NOTES:

MicroSiP is a trademark of Texas Instruments

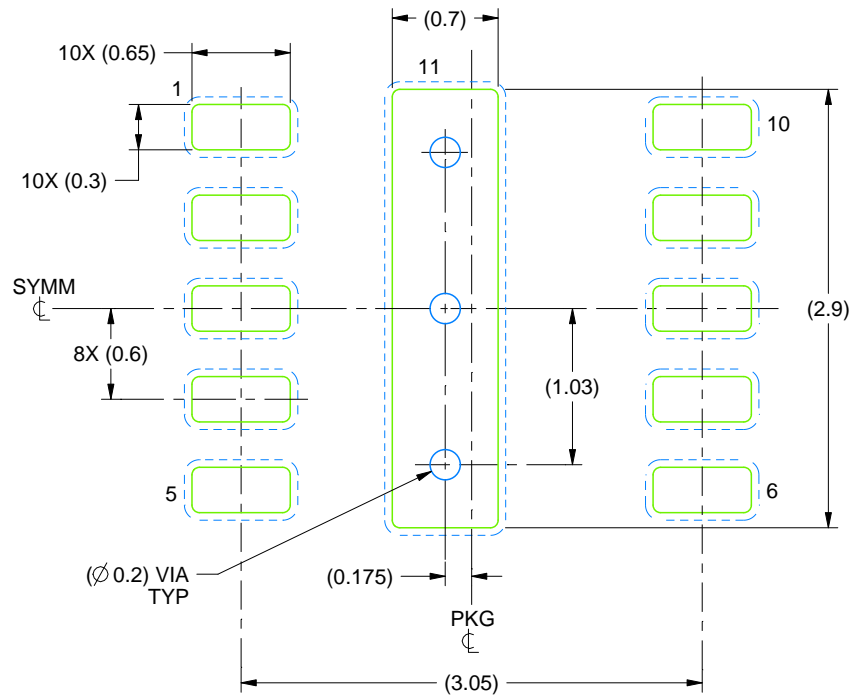
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Pick and place nozzle \varnothing 1.1 mm or smaller recommended.
4. Location, size and quantity of components are for reference only and could vary.
5. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

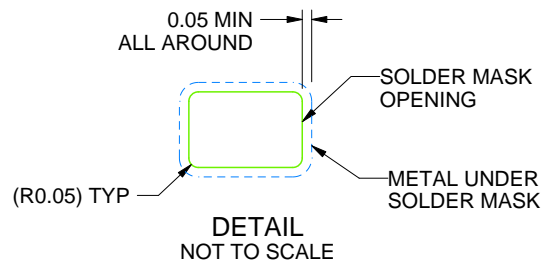
SIL0010A

MicroSiP™ - 1.578 mm max height

MICRO SYSTEM IN PACKAGE



LAND PATTERN EXAMPLE
1:1 RATIO WITH PACKAGE SOLDER PADS
SOLDER MASK DEFINED
SCALE:20X



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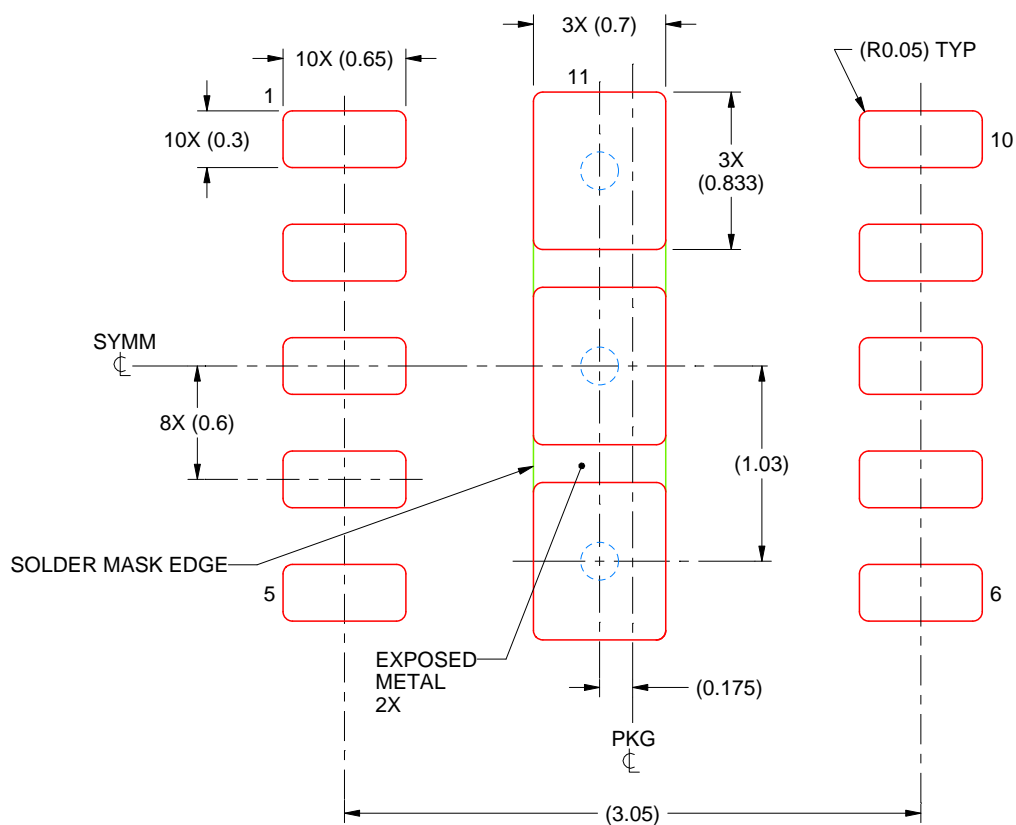
NOTES: (continued)

6. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
7. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

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MICRO SYSTEM IN PACKAGE



SOLDER PASTE EXAMPLE BASED ON 0.125 mm THICK STENCIL

PAD 11:
86% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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